
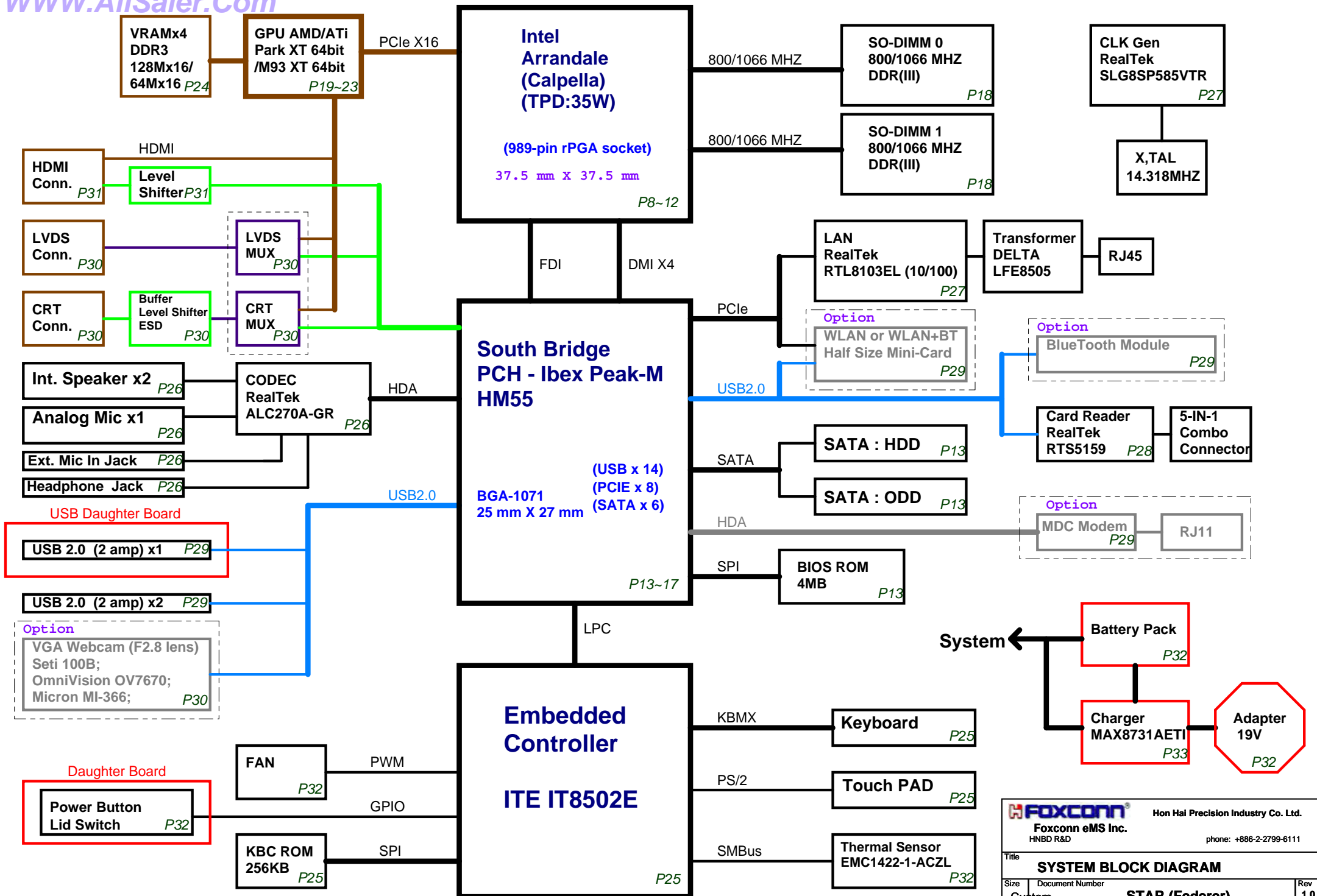


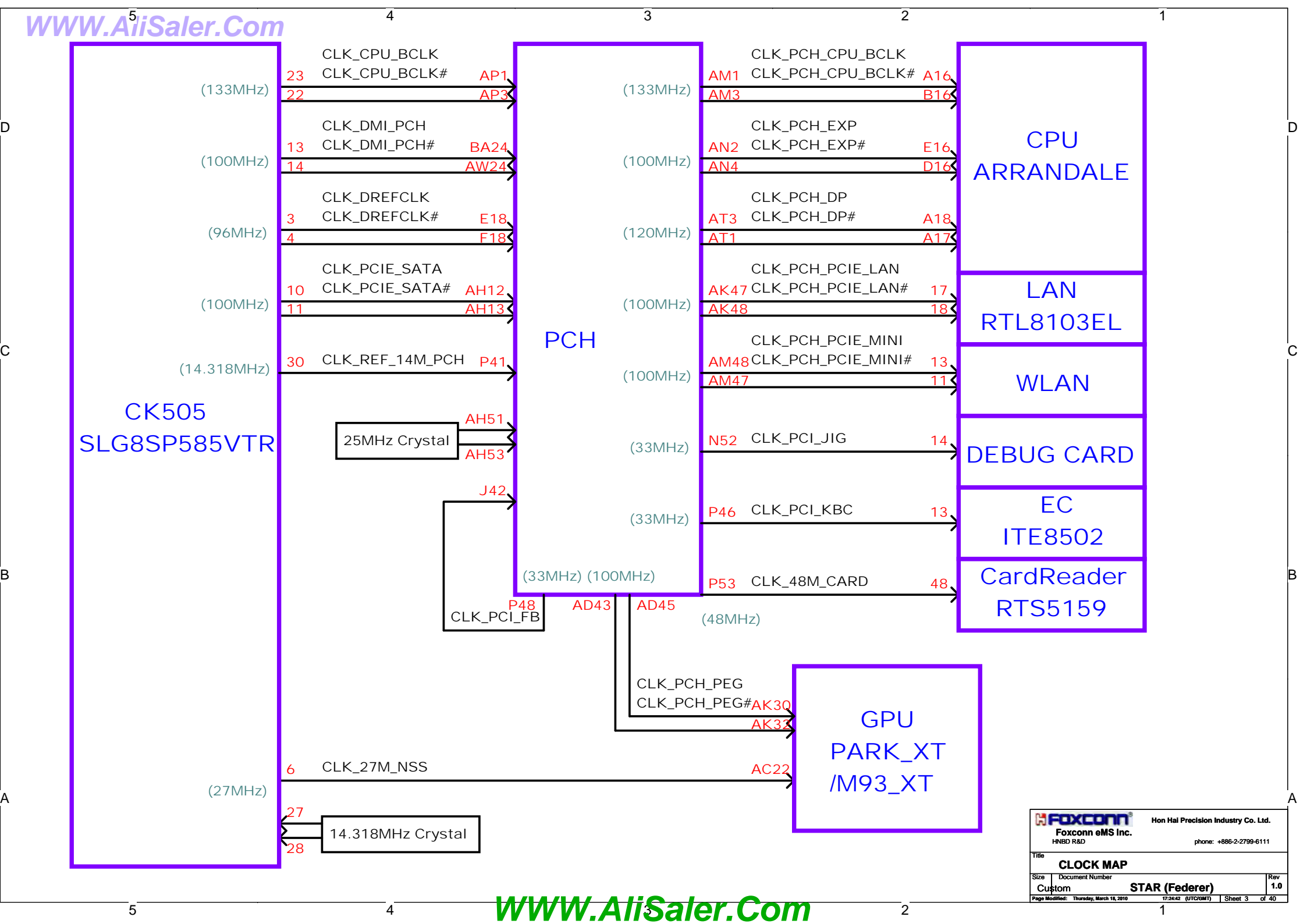
01 -- COVER SHEET	21 -- VGA_S3 (DDR3) 3/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DP) 4/5
03 -- CLOCK MAP	23 -- VGA_S3 (POWER) 5/5
04 -- POWER MAP	24 -- VRAM (DDR3)
05 -- POWER SEQUENCY DIAGRAM	25 -- EC+KBC (IT8502E)
06 -- POWER SEQUENCY TIMING	26 -- CODEC/JACK/SPEAKER/MIC
07 -- SMBUS MAP	27 -- LAN (RTL8103EL)/CLOCK GEN
08 -- Calpella (DMI,PEG,FDI)	28 -- Card Reader
09 -- Calpella (CLK,MISC,JTAG)	29 -- WLAN/BT/MDC/USB/MOUNTING
10 -- Calpella (DDR3)	30 -- LVDS/CRT/Webcam
11 -- Calpella (POWER/GND)	31 -- HDMI
12 -- Calpella (GRAPHIC POWER)	32 -- DCIN/Battery/OCP/FAN
13 -- PCH (HDA,JTAG,SATA)	33 -- PWR_Charger MAX8731AETI
14 -- PCH (PCI-E,SMBUS,CLK)	34 -- 5V/3.3V SN0608098RHBT
15 -- PCH (DMI,FDI,GPIO,LVDS)	35 -- Vcore MAX17030
16 -- PCH (PCI,USB,NVRAM,GPIO)	36 -- 1.1V VTT/+V1.05RUN
17 -- PCH (POWER)	37 -- 1.5VDDR3+0.75V+V1.8RUN
18 -- DDR3(SO-DIMM_0&1)	38 -- PWR_Others power plane
19 -- VGA (PCI-E/STRAP) 1/5	39 -- CPU VREG & Decoupling
20 -- VGA_S3 (IO) 2/5	40 -- ATVDD/+VPCIE

P. Leader	Check by	Design by


 Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.	
HNBD R&D	phone: +886-2-2799-6111

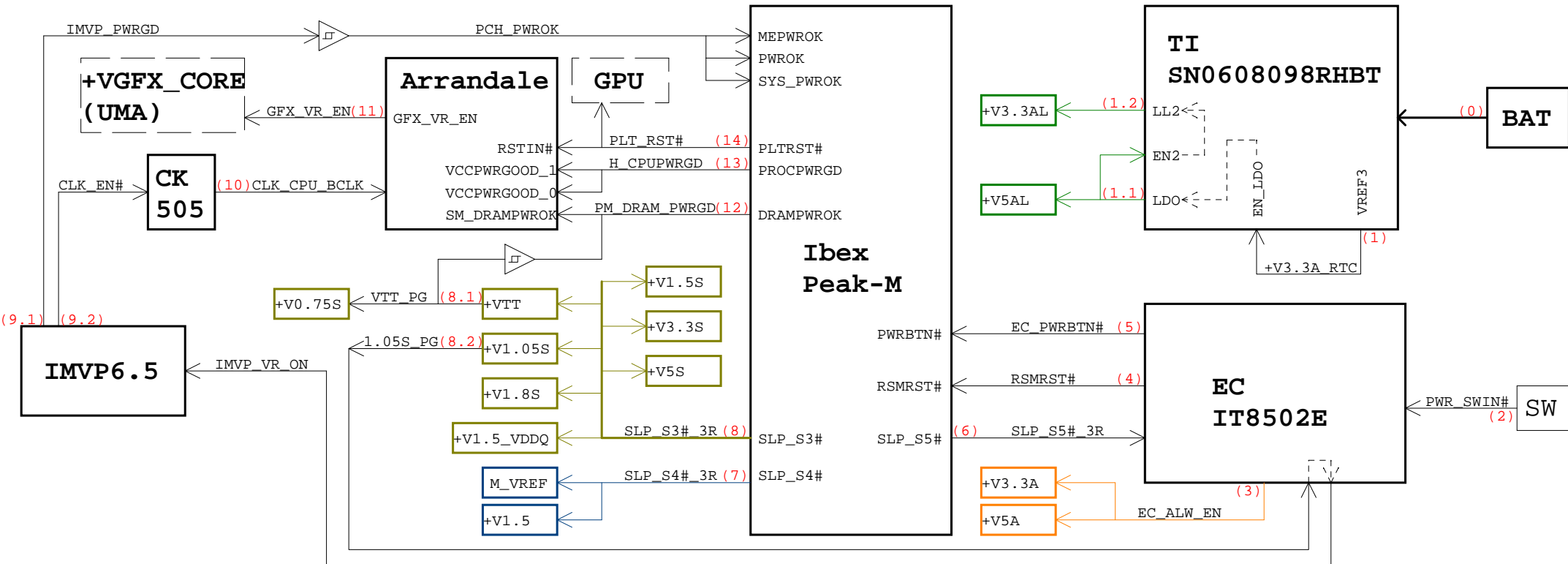
Title Index Page		
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Page Modified: Thursday, March 18, 2010 17:24:40 (UTC+GMT) Sheet 1 of 40		





SCH Page	Change Request Description	Notes
25,33~40	modify the power short pad to "POWER_OPENPAD_1P9X2P4"	SMD performance issue
15	Add RS74,RS77,RS79 for all SG sku	Fix VGA port auto detect function
39	Change PR944 from 1K to 1.5K	Fix power load line test issue
13	Del PCH SPI ROM connector circuitry	Del unnecessary functon parts
25	Del EC SPI ROM connector circuitry	Del unnecessary functon parts
25	Del debug connector	Del unnecessary function part
25	SKU ID modify to MV phase	MV Phase ID
13	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
25	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
30	VGA connector change part number to halide free type	ROHS issue
29	MDC connector change part number to halide free type	ROHS issue
29	Mini-PCIE connector change part number to halide free type	ROHS issue
30	LVDS connector change part number to halide free type	ROHS issue
13	SATA connector change part number to halide free type	ROHS issue
30	Modify backlight PWM control path	Del unnecessary parts
18	Modify the DDR3 footprint	Co-lay for DDR3 connector
25	Del D110	Del unnecessary functon parts
25,30	Del RB28 and Add RI54	For 17" keyboard num lock LED
38	add PC775	Add for GPU M93 platform
38	add PC776	Add for VGA wave issue
35	Change VCORE VDD power source from +V5A to +V5S	Modify for V-BOOT
38	Change PR769 pull high power source from +12A to +V5A	Modify for GPU power sequence
29	Modify the HOLE1006 footprint	update footprint
40	modify all VDDCORE circuitry	modify VDDCORE circuitry
26	modify UA3 pin2 Analogy GND to Digital GND	Analogy GND change to Digital GND
32	add 2 pcs 2N7002 and swap EC_CHAR_LED#_A & EC_AC_LED#_A	Modify LED control and brightness
32	modify HEADER10 pin1 power source from +V5A to +V3.3AL	modify LED control and brightness
33~37	PC547 22uF_X5R_25V to 10uF_X5R_25V*2	modify for acoustic
	PC504 4.7uF_X5R_25V to 10uF_X5R_25V	
	PC813 4.7uF_X5R_25V to 10uF_X5R_25V	
	PC825, PC812 to 10uF_X5R_25V (NI)	
	PC826 to 10uF_X5R_25V (NI)	
	PC824, PC828, PC829 4.7uF_X5R_25V to 10uF_X5R_25V"	
32	RH1002 change to 1.3Kohm	modify LED control and brightness
27	RL13 change to 2.7Kohm"	modify LED control and brightness
32	ADD QB11	Thermal shutdown
19	ADD RG457,RG458	Add for power leakage issue
35	Del DB14	Thermal shutdown issue

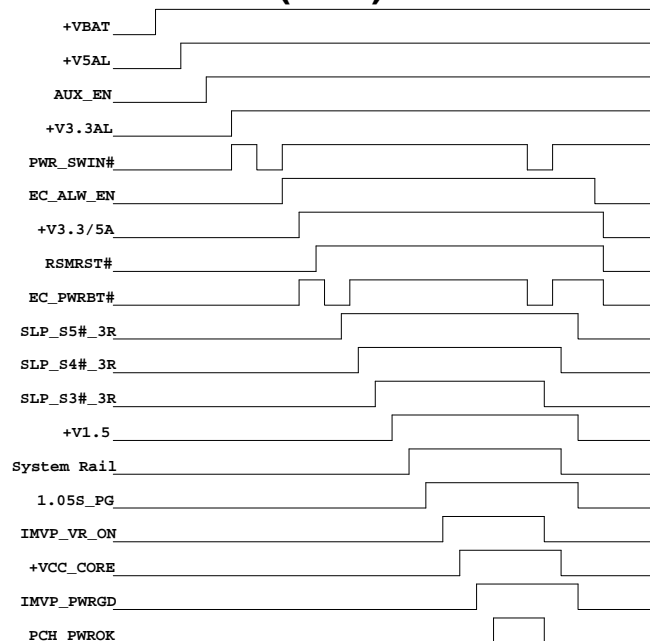
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History			
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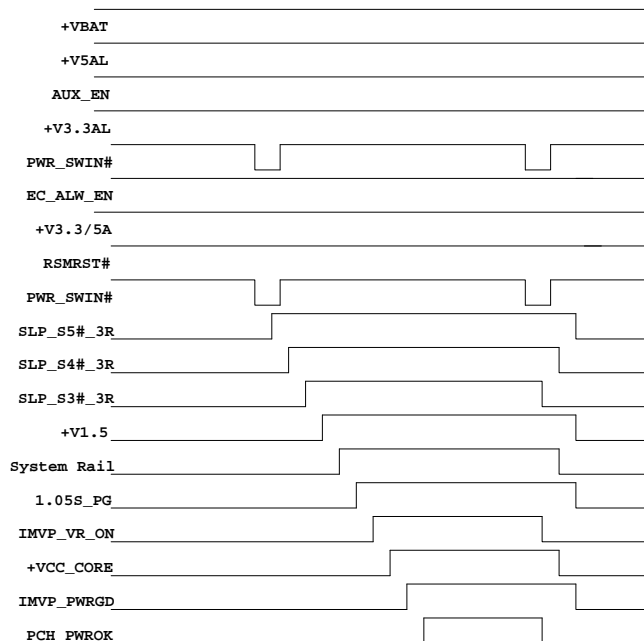
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT	+VBAT	+V3.3A_RTC		V	V	V	V	
+V5AL	+VBAT	+V5AL		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+VBAT	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

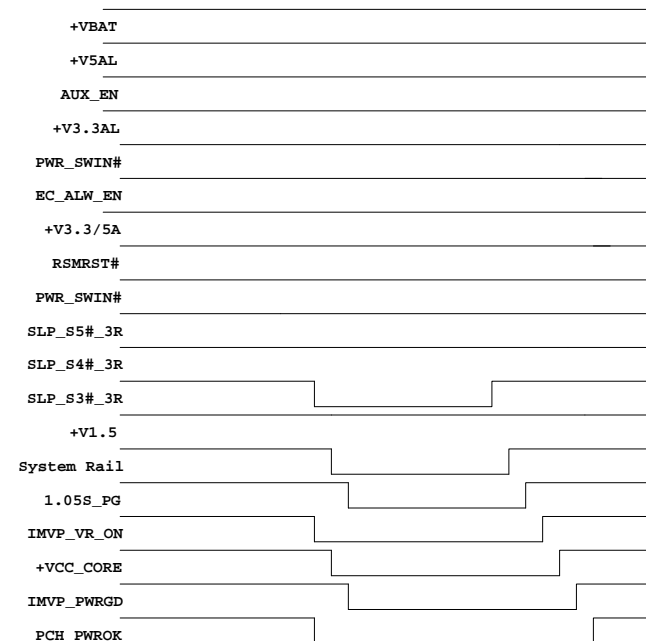
G3(OFF)->S0->S5



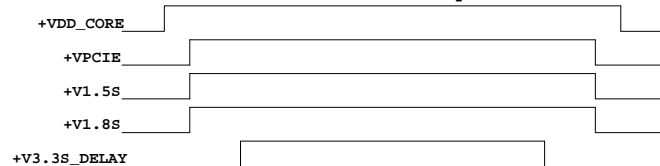
S5->S0->S5



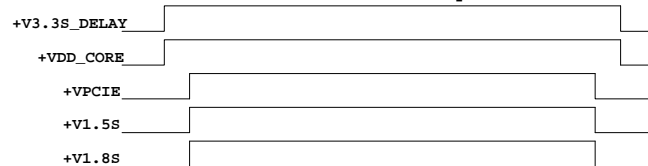
S0->S3->S0



GPU_M93 Sequence



GPU_Park Sequence



Switchable GPU

GPU
Park_XT

PCH

EC
ITE8502

DIMM0

DIMM1

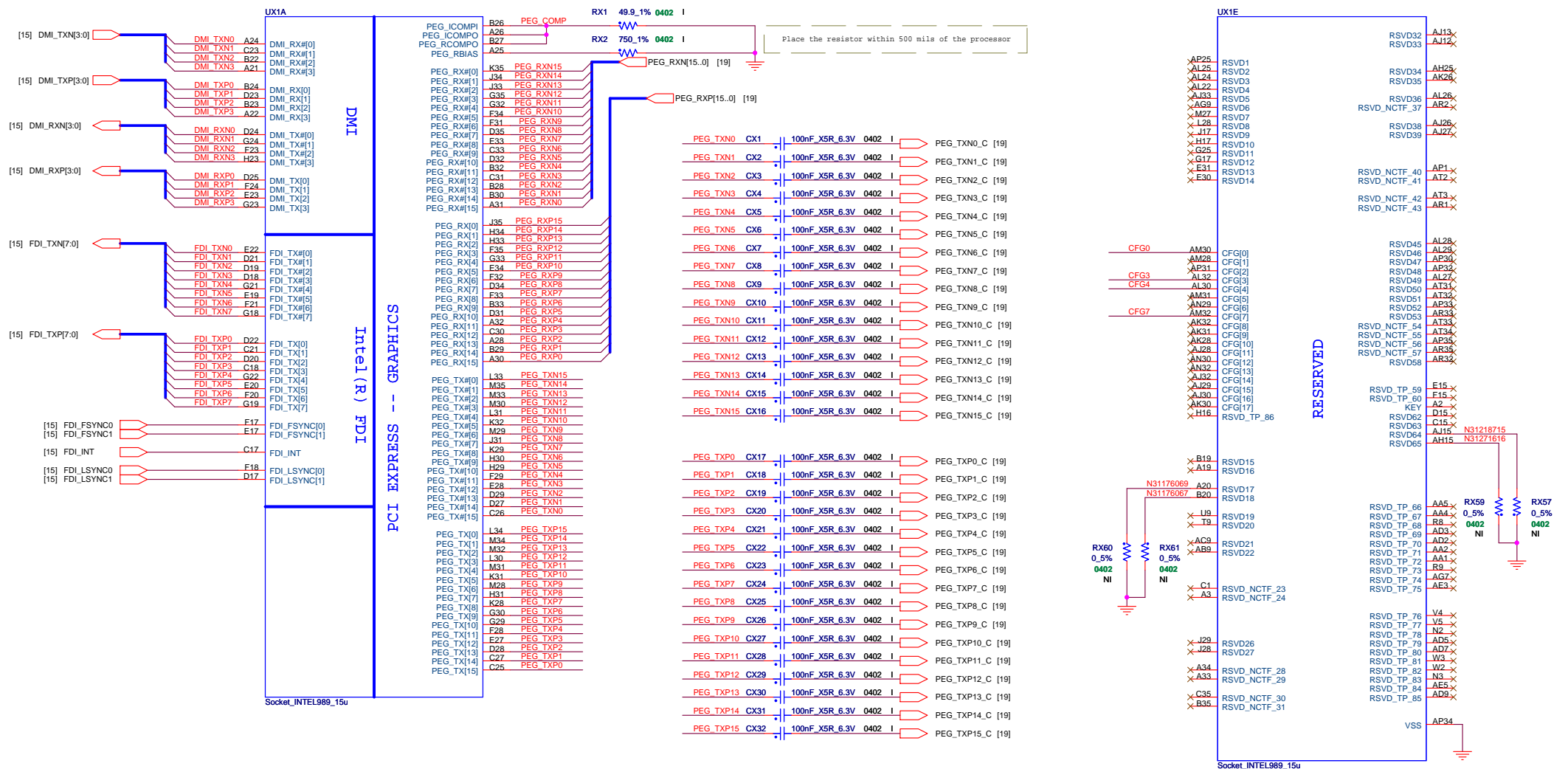
CLOCK
GEN

WLAN

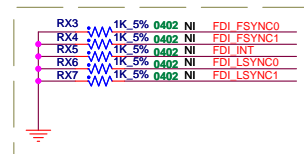
Temp
Sensor

Charger

Battery



Discrete GPU: Install
UMA: Not Install



CFG4 Display Port Presence
1 : Disabled ; No Physical Display Port
attached to Embedded Display Port
0 : Enable ; An external Display Port device
is connected to the Embedded Display Port

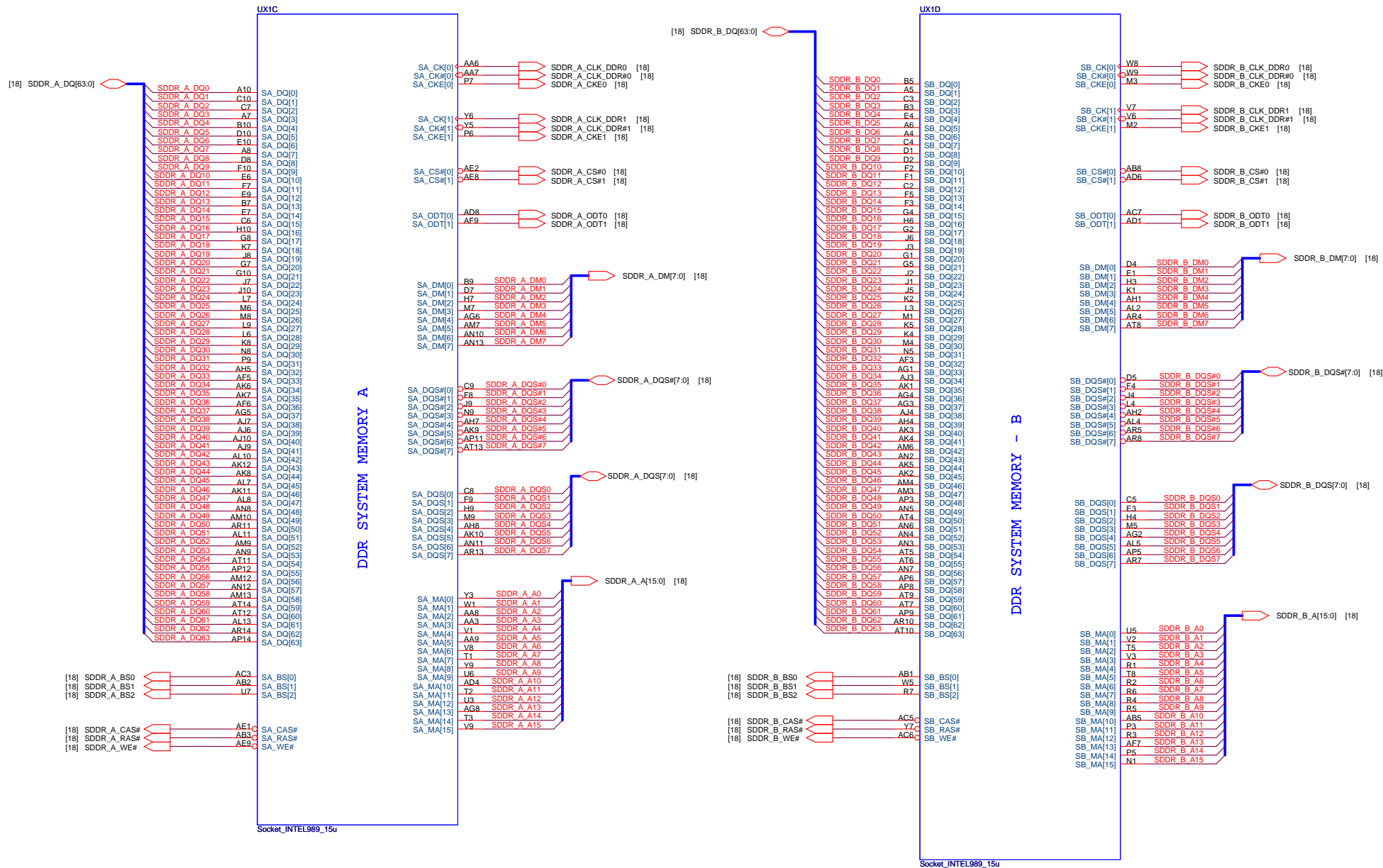
CFG7 Reserved - Temporarily used for early Clarkfield samples.
Clarkfield (only for early samples pre-E31) -
Connect to GND with 3.01K Ohm/5% resistor

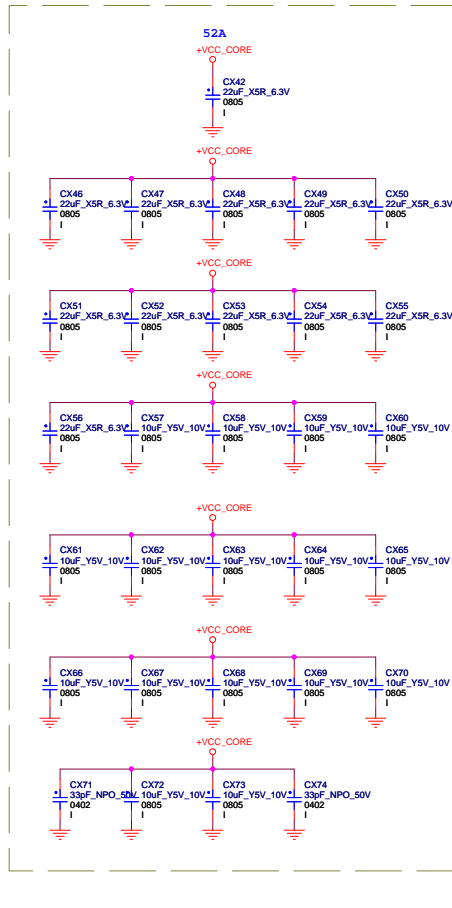
PCI Express Configuration Select
CFG0
1 : Single PEG
0 : Bifurcation enabled

CFG3 PCI Express Static Lane Reversal
CFG3
1 : Normal Operation
0 : Lane Numbers Reversed
15 -> 0 , 14 -> 1 , ...

Clarksfield: 1.1V(RX38=1.1K 1%; RX43=3.01K 1%)	Clarksfield: 1.1V(RX41=2K 1%; RX44=1K 1%)
Arrandale : 1.05V(RX38=1.1K 1% ; Rx43=2.61K 1%)	Arrandale : 1.05V(RX41=2K 1% ; R44=931ohm 1%)

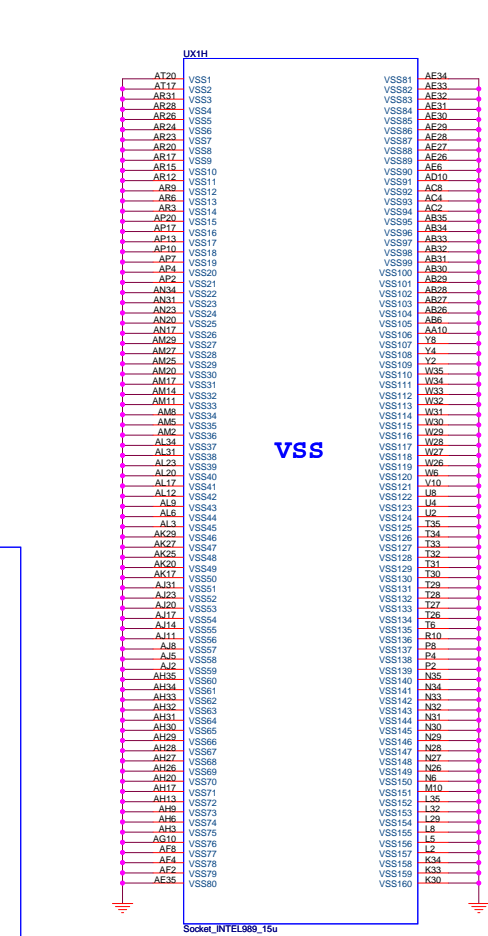
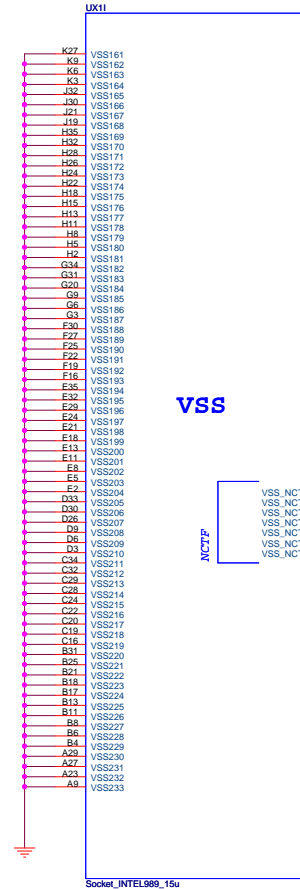
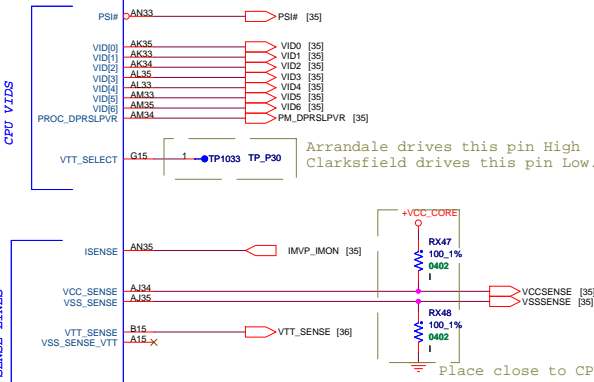
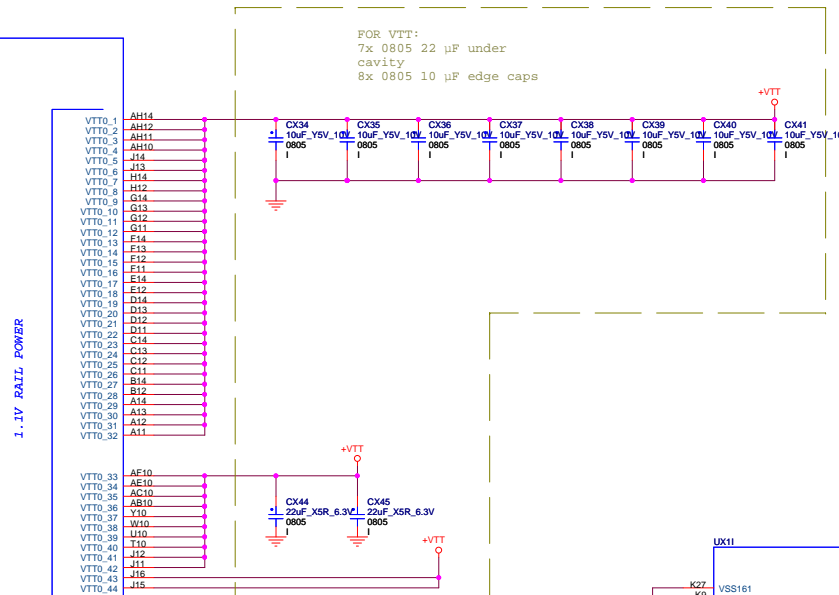


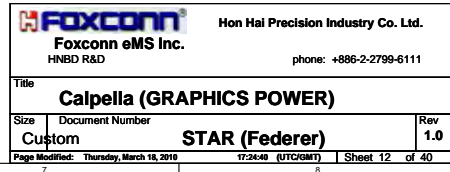


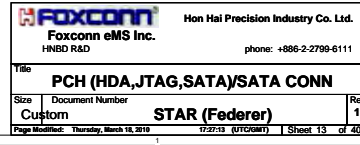


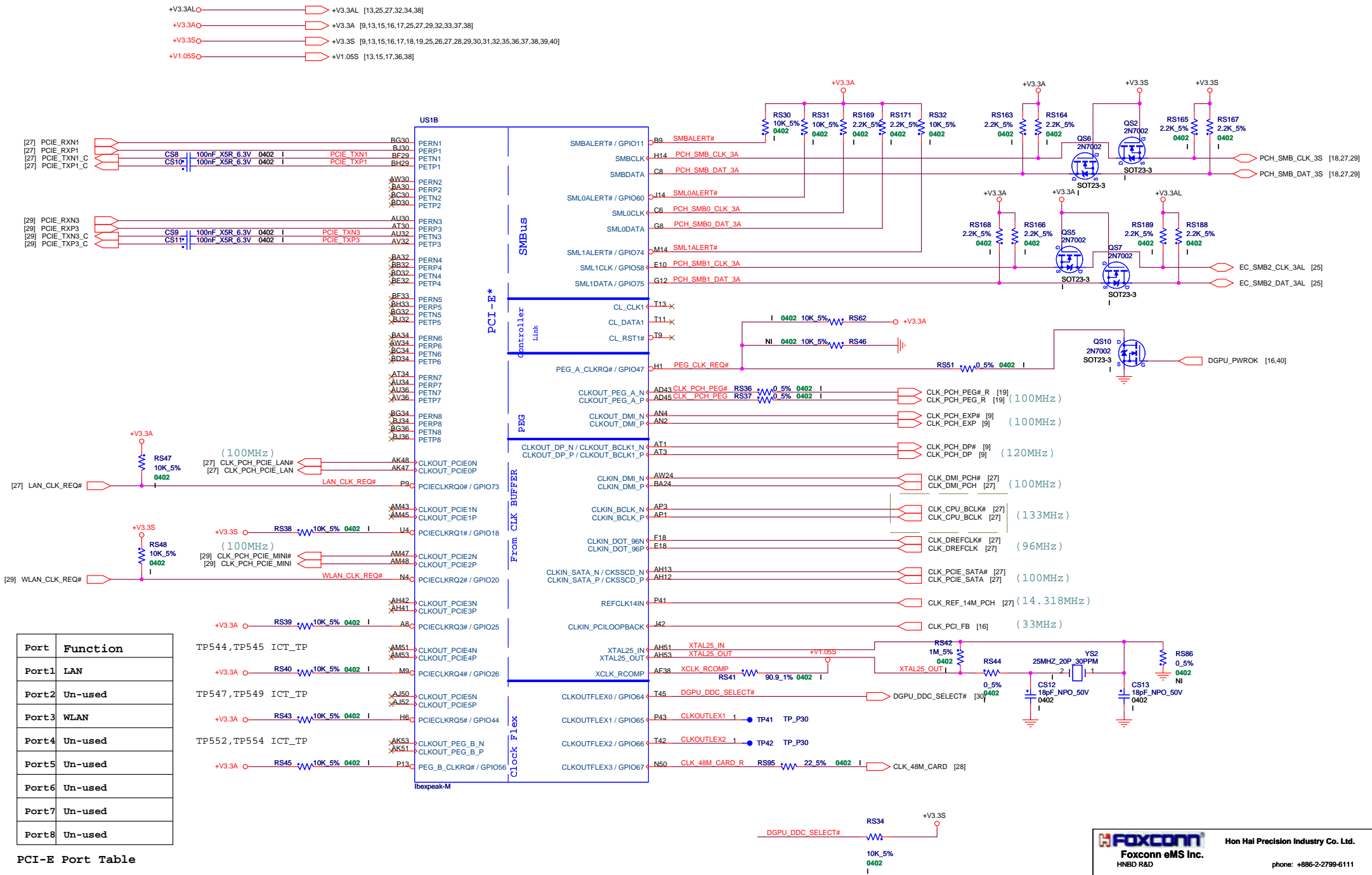
Socket_INTEL989_15u

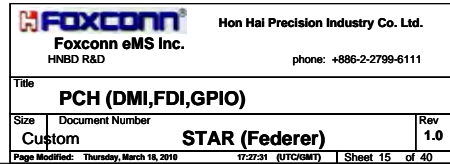
FOR VTT:
7x 0805 22 μ F under
cavity
8x 0805 10 μ F edge caps

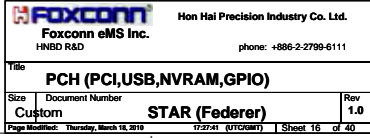




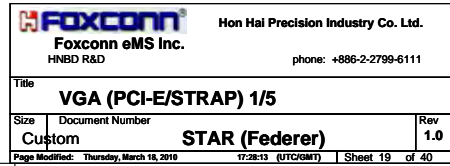


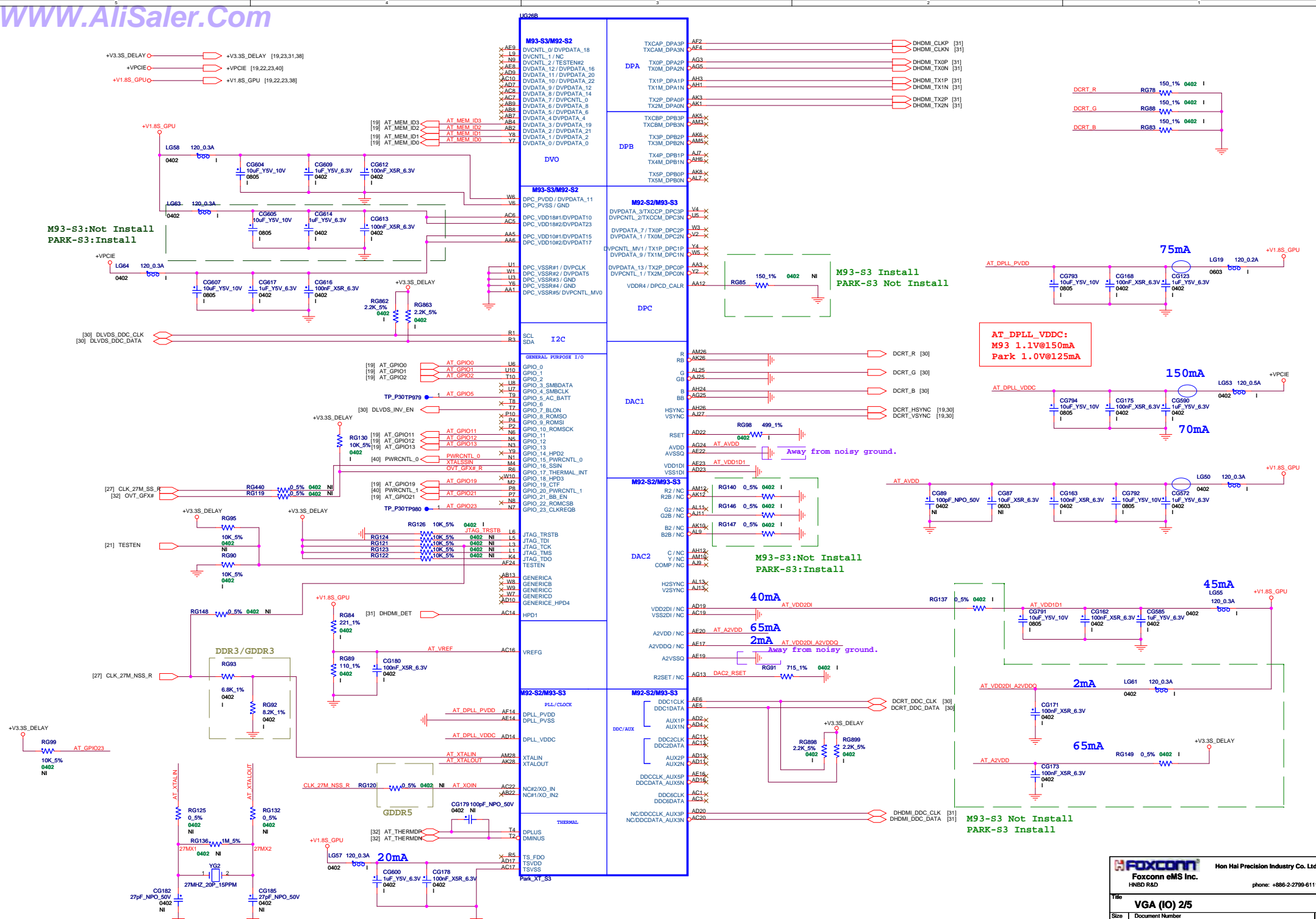


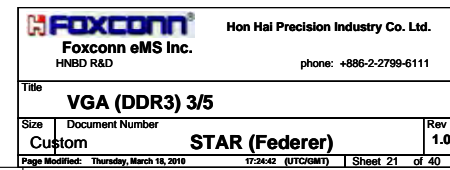


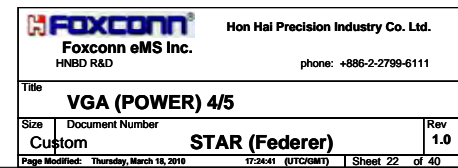


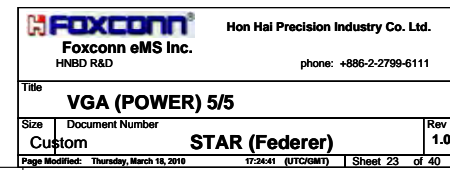




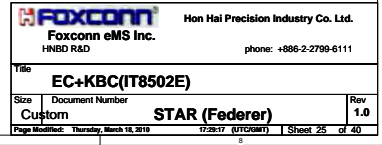


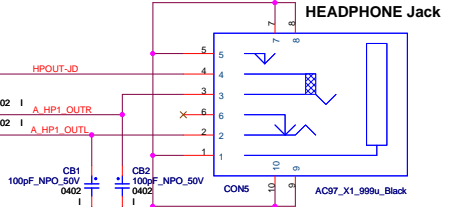
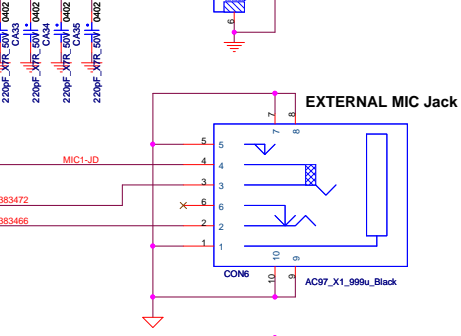
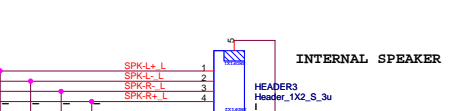
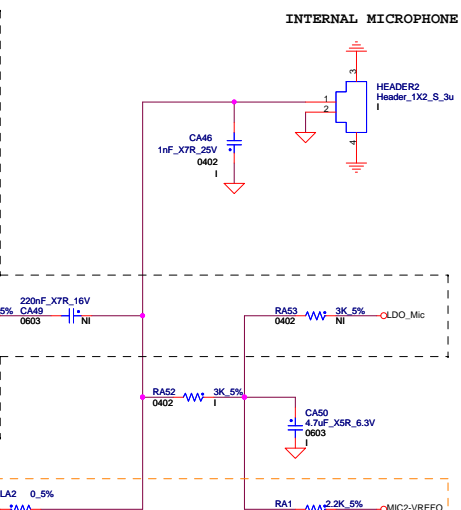
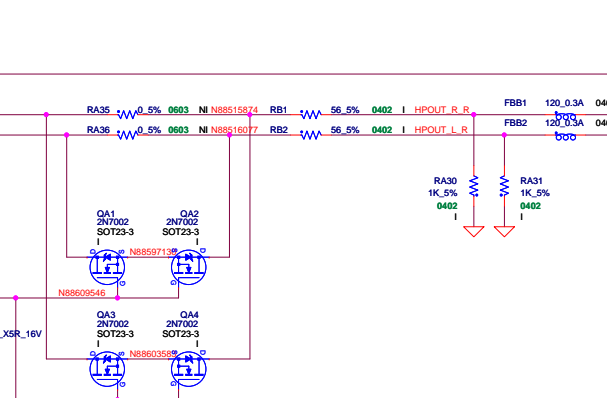
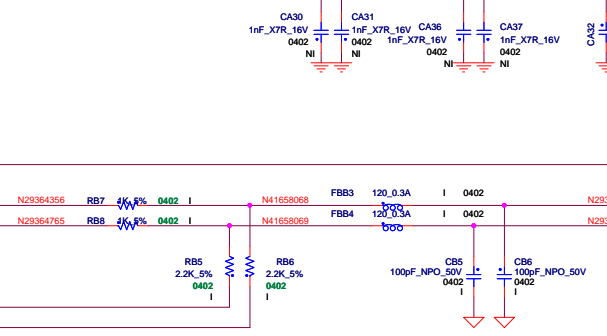
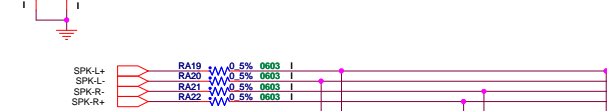
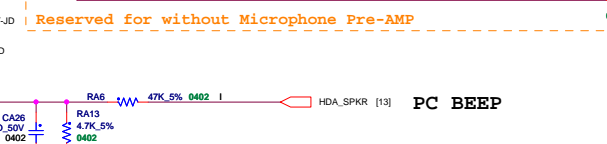
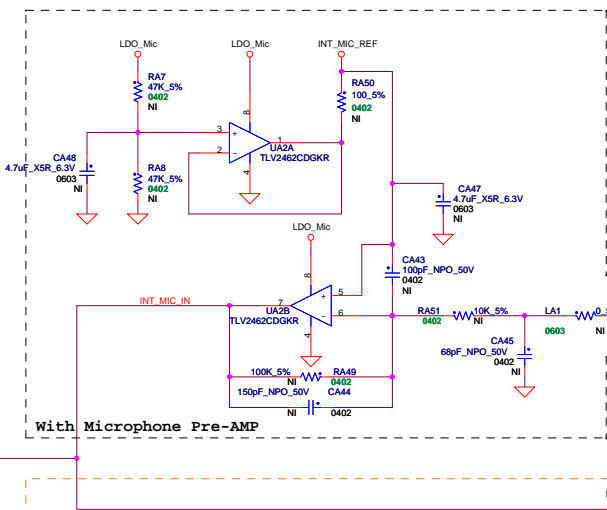
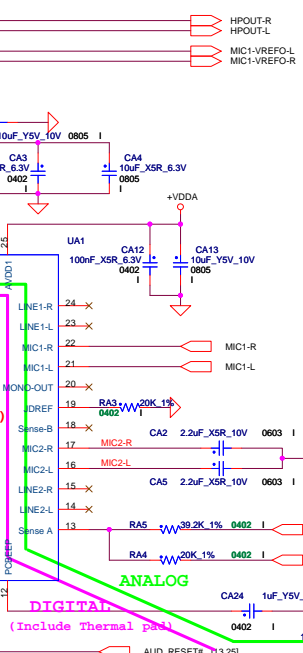
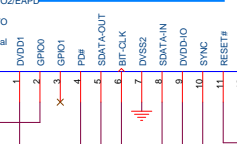
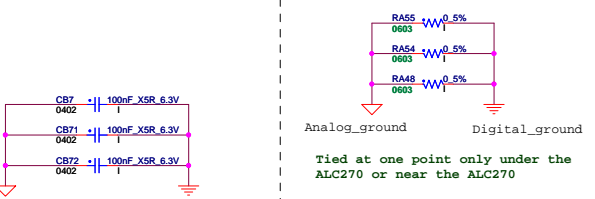
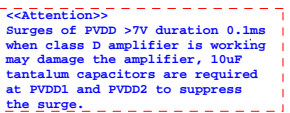
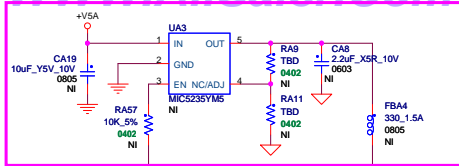








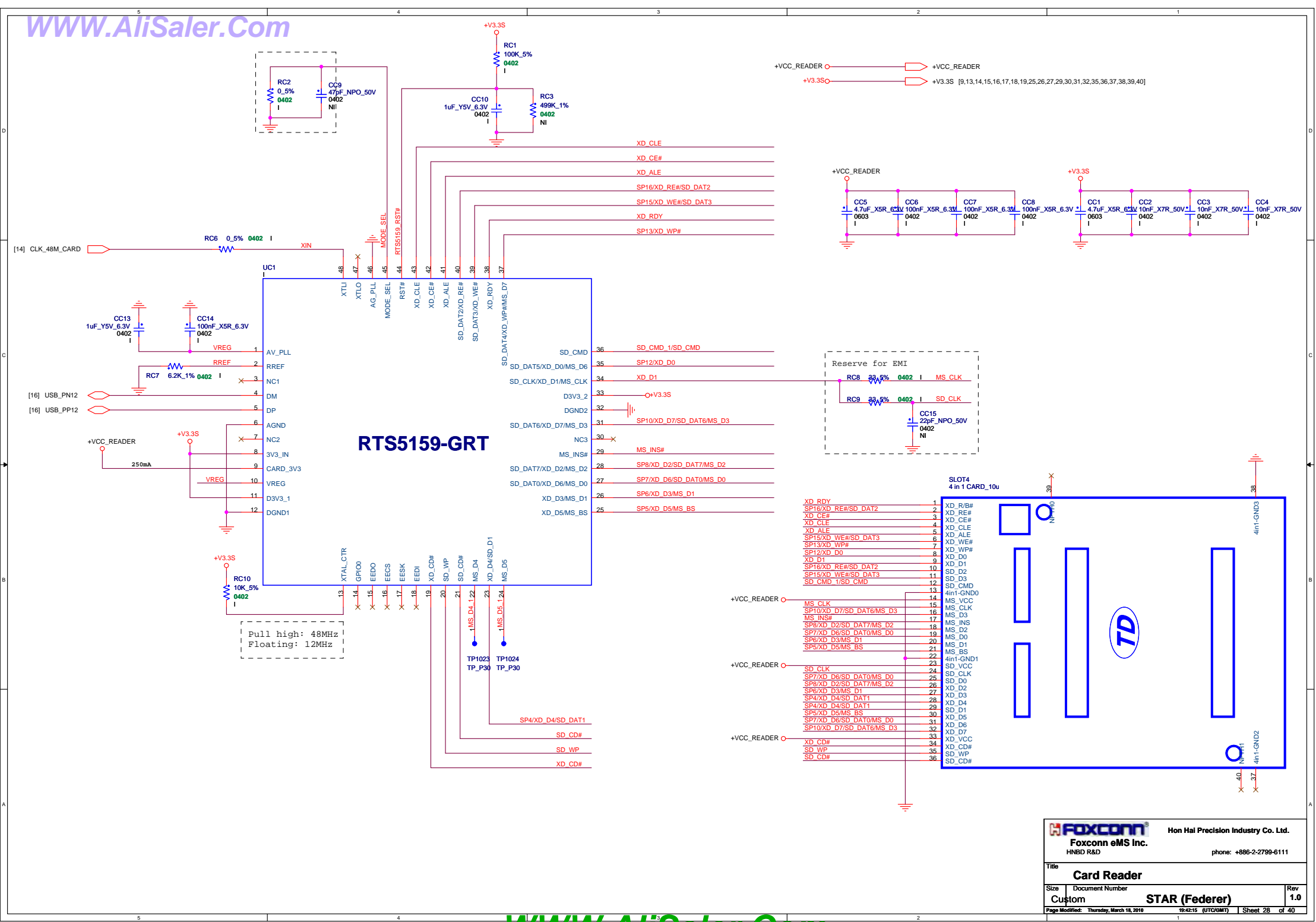


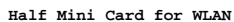




FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

1.0





MDC CONN.



Bluetooth CONN.

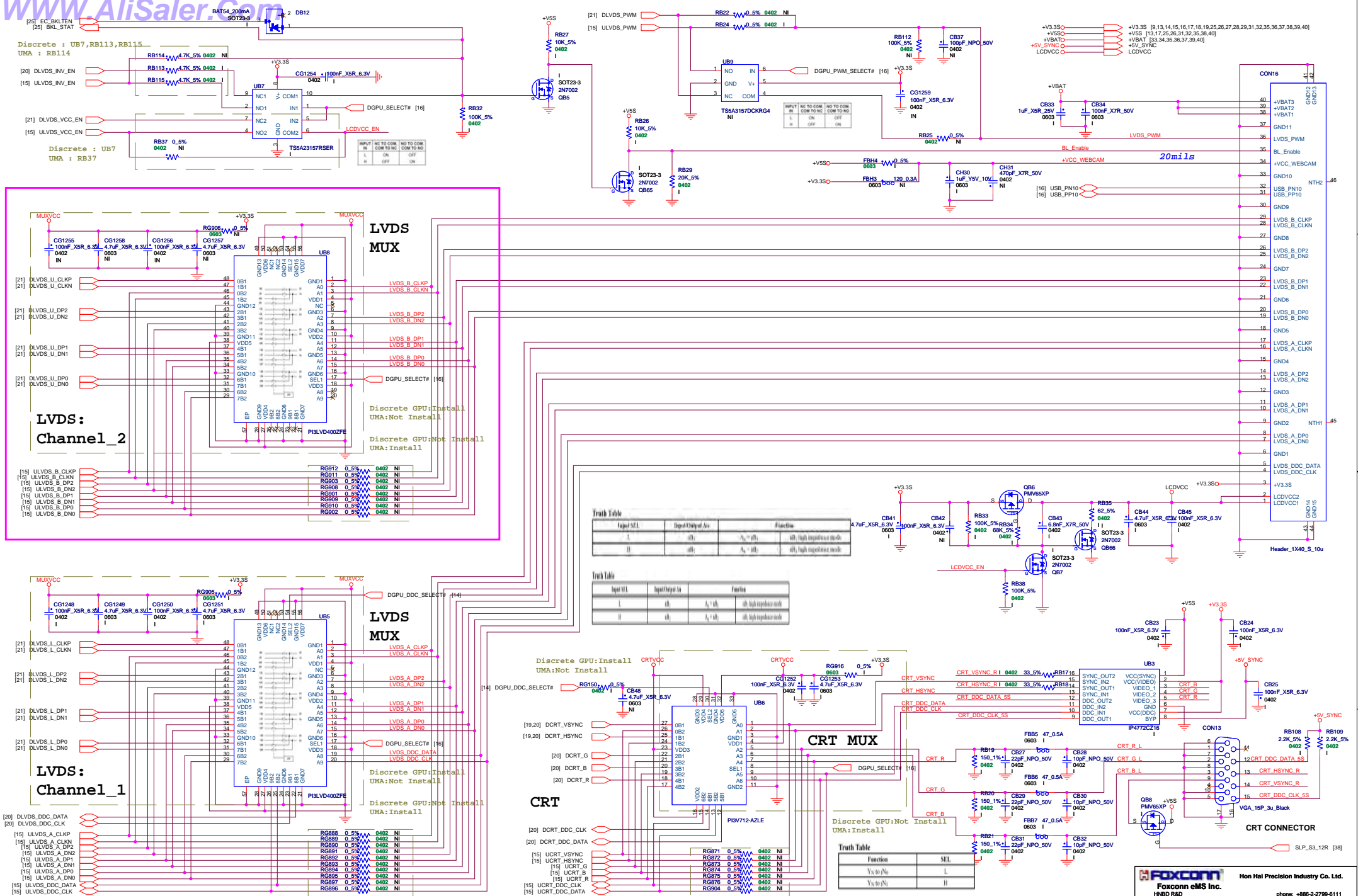


USBX2 CONN.

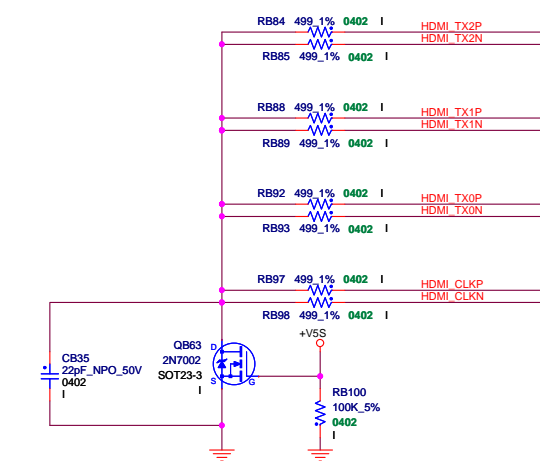
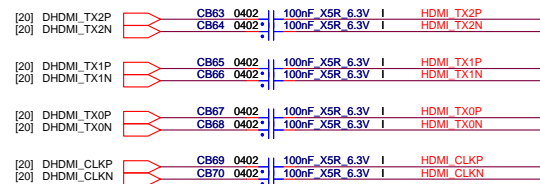
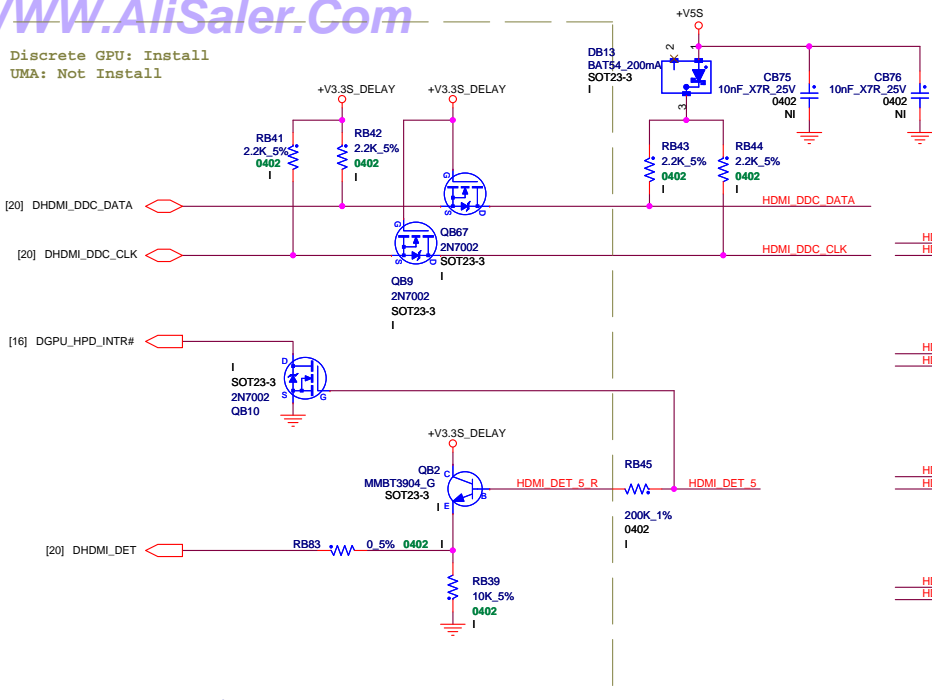
MOUNTING
HOLE

USBX1 CONN.

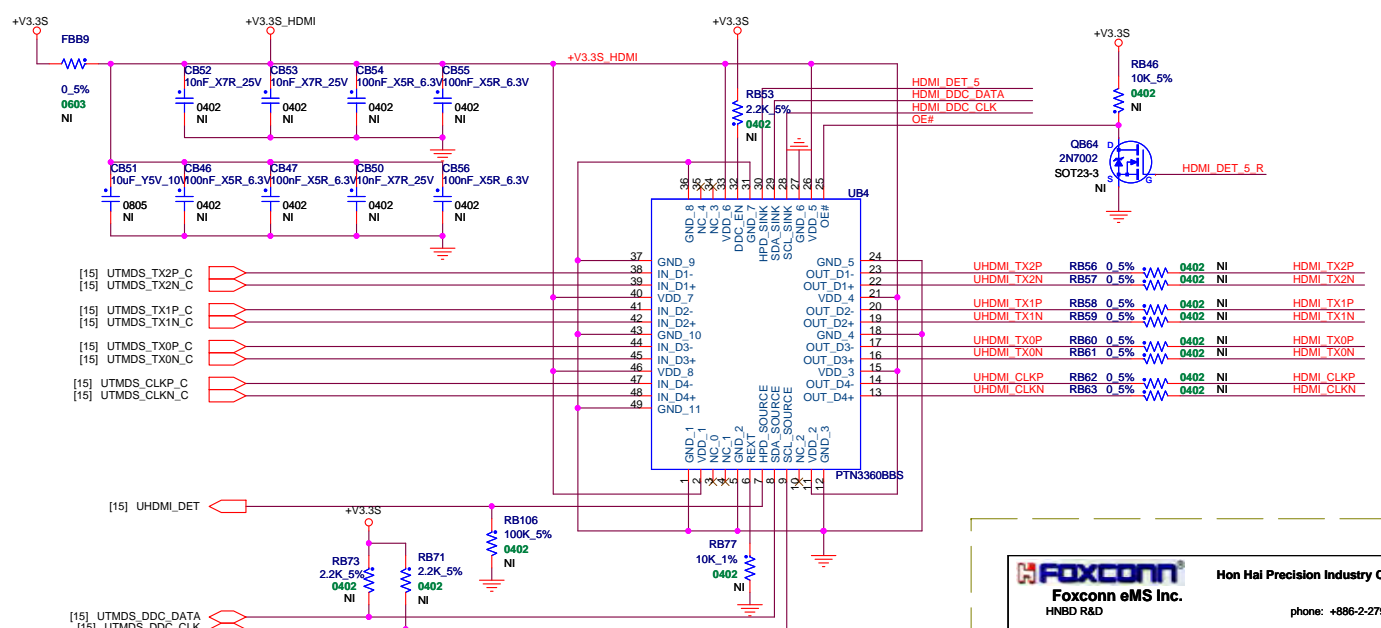




Discrete GPU: Install
UMA: Not Install



Discrete GPU:Not Install
UMA:Install



HDMI spec:
+5V: 4.7V min,
55mA max.

POWER BUTTON BOARD CONNECTOR

DC_JACK Wire to Board Connector

DC_JACK Wire to Board Connector

Diagram illustrating the wiring for the DC_JACK Wire to Board Connector. The connector is labeled ADAPTOR In CON. and is connected to a 7-pin header (SLOT9).

The wiring connections are as follows:

- Pin 1 (DC+) connects to +V3.3A.
- Pin 2 (GND) connects to GND.
- Pin 3 (GND) connects to GND.
- Pin 4 (GND) connects to GND.
- Pin 5 (GND) connects to GND.
- Pin 6 (GND) connects to GND.
- Pin 7 (GND) connects to GND.

The +V3.3A line is filtered with a 100nF capacitor (CB61) and a 100nF capacitor (CB62). The GND line is filtered with a 10nF capacitor (CB77) and a 10nF capacitor (CB78). The output is connected to EC_CHAR_LED#_A [25] and EC_AC_LED#_W [25].

THERMAL SENSOR

W/S:10/10 (microstrip)

[20] AT_THERMDP

[20] AT_THERMDIN

CH27 2.2nF_XTR_50V 0402

CH29 100nF_XSR_6.3V 0402

CH32 100nF_XSR_6.3V 0402

CH23 100nF_XSR_6.3V 0402

CH24 29.4k_1% 0402

CH25 100k_5% 0402

CH26 15k_1% 0402

CH28 33k_1% 0402

CH30 2M_5% 0402

CH31 330_5% 0803

CH33 150_1% 0402

CH34 2N7002 SOT23-3

CH35 2N7002 SOT23-3

CH36 2N7002 SOT23-3

CH37 2N7002 SOT23-3

CH38 2N7002 SOT23-3

CH39 2N7002 SOT23-3

CH40 2N7002 SOT23-3

CH41 2N7002 SOT23-3

CH42 2N7002 SOT23-3

CH43 2N7002 SOT23-3

CH44 2N7002 SOT23-3

CH45 2N7002 SOT23-3

CH46 2N7002 SOT23-3

CH47 2N7002 SOT23-3

CH48 2N7002 SOT23-3

CH49 2N7002 SOT23-3

CH50 2N7002 SOT23-3

CH51 2N7002 SOT23-3

CH52 2N7002 SOT23-3

CH53 2N7002 SOT23-3

CH54 2N7002 SOT23-3

CH55 2N7002 SOT23-3

CH56 2N7002 SOT23-3

CH57 2N7002 SOT23-3

CH58 2N7002 SOT23-3

CH59 2N7002 SOT23-3

CH60 2N7002 SOT23-3

CH61 2N7002 SOT23-3

CH62 2N7002 SOT23-3

CH63 2N7002 SOT23-3

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CH65 2N7002 SOT23-3

CH66 2N7002 SOT23-3

CH67 2N7002 SOT23-3

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CH70 2N7002 SOT23-3

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CH75 2N7002 SOT23-3

CH76 2N7002 SOT23-3

CH77 2N7002 SOT23-3

CH78 2N7002 SOT23-3

CH79 2N7002 SOT23-3

CH80 2N7002 SOT23-3

CH81 2N7002 SOT23-3

CH82 2N7002 SOT23-3

CH83 2N7002 SOT23-3

CH84 2N7002 SOT23-3

CH85 2N7002 SOT23-3

CH86 2N7002 SOT23-3

CH87 2N7002 SOT23-3

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CH90 2N7002 SOT23-3

CH91 2N7002 SOT23-3

CH92 2N7002 SOT23-3

CH93 2N7002 SOT23-3

CH94 2N7002 SOT23-3

CH95 2N7002 SOT23-3

CH96 2N7002 SOT23-3

CH97 2N7002 SOT23-3

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CH100 2N7002 SOT23-3

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CH104 2N7002 SOT23-3

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CH119 2N7002 SOT23-3

CH120 2N7002 SOT23-3

CH121 2N7002 SOT23-3

CH122 2N7002 SOT23-3

CH123 2N7002 SOT23-3

CH124 2N7002 SOT23-3

CH125 2N7002 SOT23-3

CH126 2N7002 SOT23-3

CH127 2N7002 SOT23-3

CH128 2N7002 SOT23-3

CH129 2N7002 SOT23-3

CH130 2N7002 SOT23-3

CH131 2N7002 SOT23-3

CH132 2N7002 SOT23-3

CH133 2N7002 SOT23-3

CH134 2N7002 SOT23-3

CH135 2N7002 SOT23-3

CH136 2N7002 SOT23-3

CH137 2N7002 SOT23-3

CH138 2N7002 SOT23-3

CH139 2N7002 SOT23-3

CH140 2N7002 SOT23-3

CH141 2N7002 SOT23-3

CH142 2N7002 SOT23-3

CH143 2N7002 SOT23-3

CH144 2N7002 SOT23-3

CH145 2N7002 SOT23-3

CH146 2N7002 SOT23-3

CH147 2N7002 SOT23-3

CH148 2N7002 SOT23-3

CH149 2N7002 SOT23-3

CH150 2N7002 SOT23-3

CH151 2N7002 SOT23-3

CH152 2N7002 SOT23-3

CH153 2N7002 SOT23-3

CH154 2N7002 SOT23-3

CH155 2N7002 SOT23-3

CH156 2N7002 SOT23-3

CH157 2N7002 SOT23-3

CH158 2N7002 SOT23-3

CH159 2N7002 SOT23-3

CH160 2N7002 SOT23-3

CH161 2N7002 SOT23-3

CH162 2N7002 SOT23-3

CH163 2N7002 SOT23-3

CH164 2N7002 SOT23-3

CH165 2N7002 SOT23-3

CH166 2N7002 SOT23-3

CH167 2N7002 SOT23-3

CH168 2N7002 SOT23-3

CH169 2N7002 SOT23-3

CH170 2N7002 SOT23-3

CH171 2N7002 SOT23-3

CH172 2N7002 SOT23-3

CH173 2N7002 SOT23-3

CH174 2N7002 SOT23-3

CH175 2N7002 SOT23-3

CH176 2N7002 SOT23-3

CH177 2N7002 SOT23-3

CH178 2N7002 SOT23-3

CH179 2N7002 SOT23-3

CH180 2N7002 SOT23-3

CH181 2N7002 SOT23-3

CH182 2N7002 SOT23-3

CH183 2N7002 SOT23-3

CH184 2N7002 SOT23-3

CH185 2N7002 SOT23-3

CH186 2N7002 SOT23-3

CH187 2N7002 SOT23-3

CH188 2N7002 SOT23-3

CH189 2N7002 SOT23-3

CH190 2N7002 SOT23-3

CH191 2N7002 SOT23-3

CH192 2N7002 SOT23-3

CH

BATTERY CONNECTOR

BT+ FBB11 60_6A 1806

BT- FBB12 60_6A 1806

+V3.3AL RB104 100K_5% 0402

RB102 100_5% 0402

RB101 100_5% 0402

RB103 100_5% 0402

CB59 100nF_Y5V_50V 0603

CB60 100nF_Y5V_50V 0603

DB19 BAV99LT1G_215mA SOT23-3

DB20 BAV99LT1G_215mA SOT23-3

DB21 BAV99LT1G_215mA SOT23-3

[25,33] EC_SMB1_DAT_3AL

[25,33] EC_SMB1_CLK_3AL

[25] BATT_THER_ALERT#

HEADER7 BT+ 1

HEADER7 SMD 2

HEADER7 SMC 3

HEADER7 SMC 4

HEADER7 THER 5

HEADER7 THER 6

HEADER7 THER 7

HEADER7 THER 8

HEADER7 THER 9

HEADER7 THER 10

HEADER7 THER 11

HEADER7 THER 12

HEADER7 THER 13

HEADER7 THER 14

HEADER7 THER 15

HEADER7 THER 16

HEADER7 THER 17

HEADER7 THER 18

HEADER7 THER 19

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HEADER7 THER 23

HEADER7 THER 24

HEADER7 THER 25

HEADER7 THER 26


HEADER7 THER 27

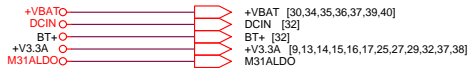
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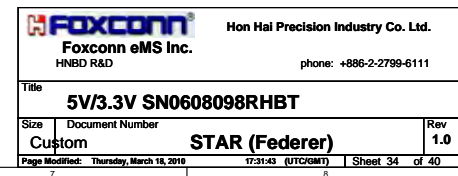
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HEADER7 THER 30

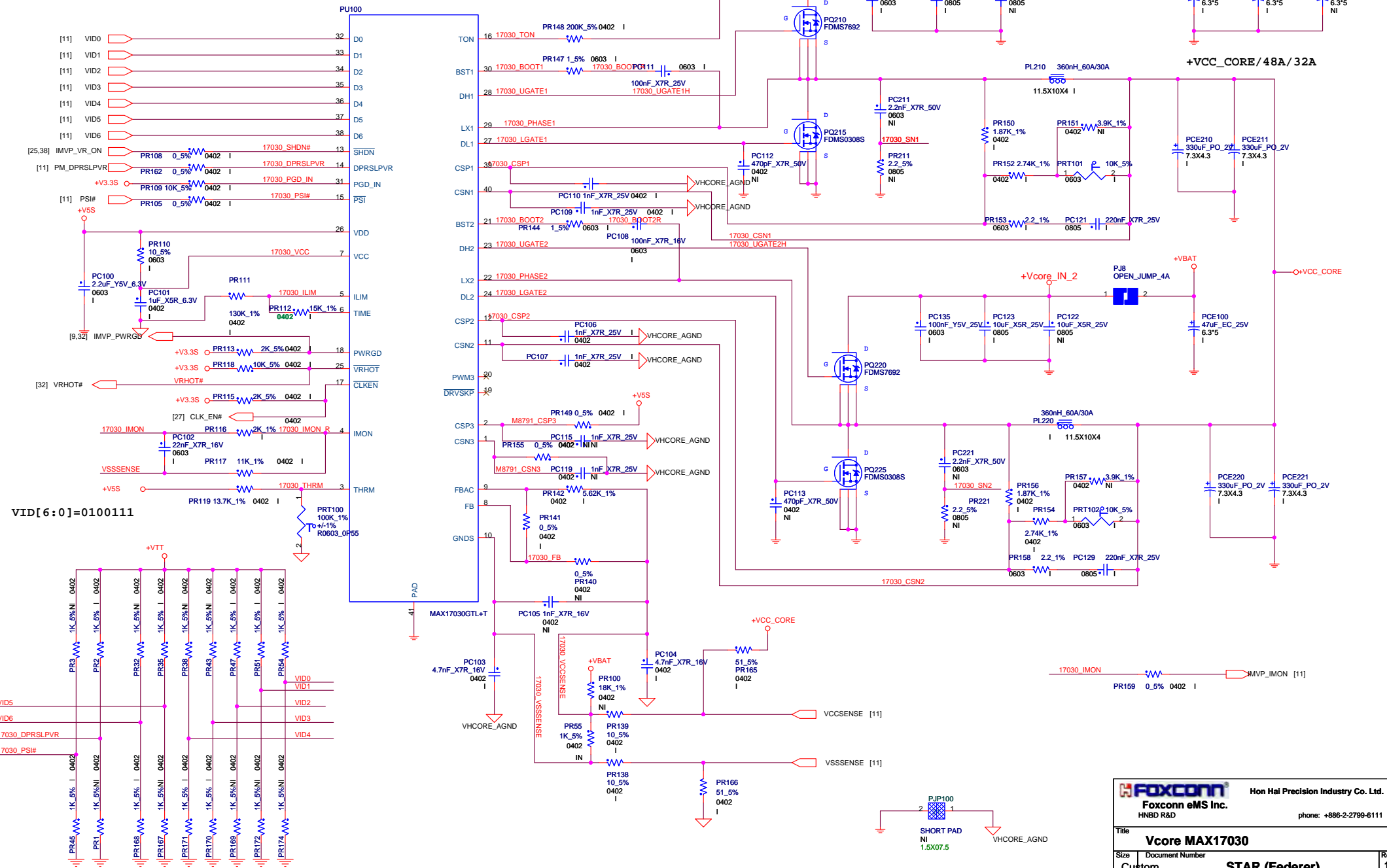
Battery_Vx8_30v_Black

		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc. HNBD R&D		phone: +886-2-2799-6111	
Title DCIN/Battery/OCF/FAN			
Size	Document Number		
Custom	STAR (Federer)		
Page Modified: Thursday, March 18, 2010		17:31:58 (UTC+08)	Sheet 32 of 44



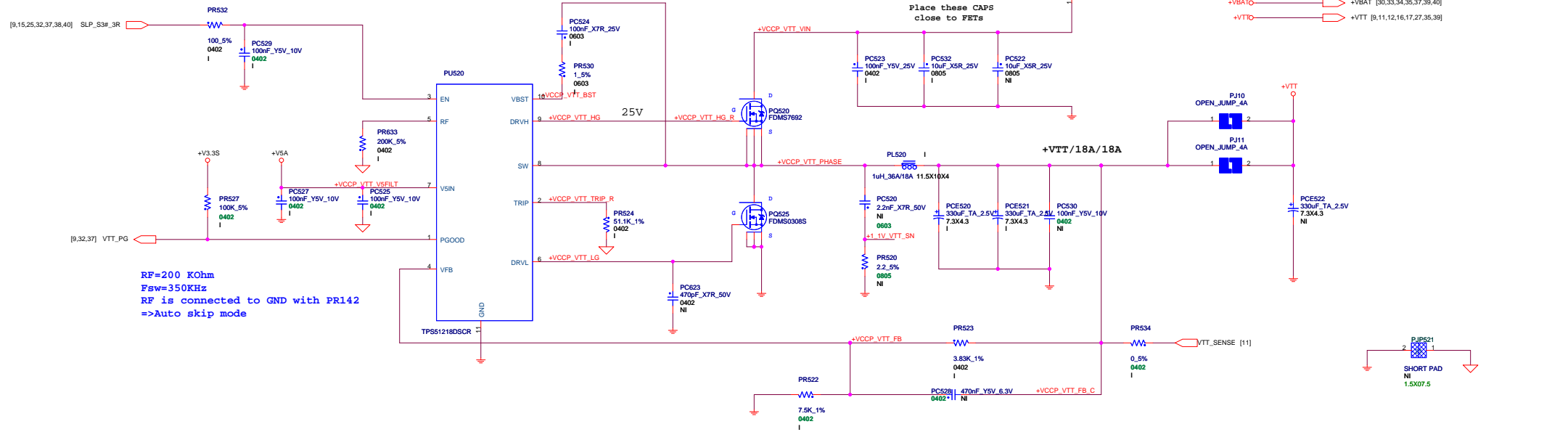


+V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,36,37,38,39,40]
 +VSS [13,17,25,26,30,31,32,38,40]
 +VBAT [30,33,34,36,37,39,40]
 +VTT [9,11,12,16,17,27,36,39]
 +VCC_CORE [11]

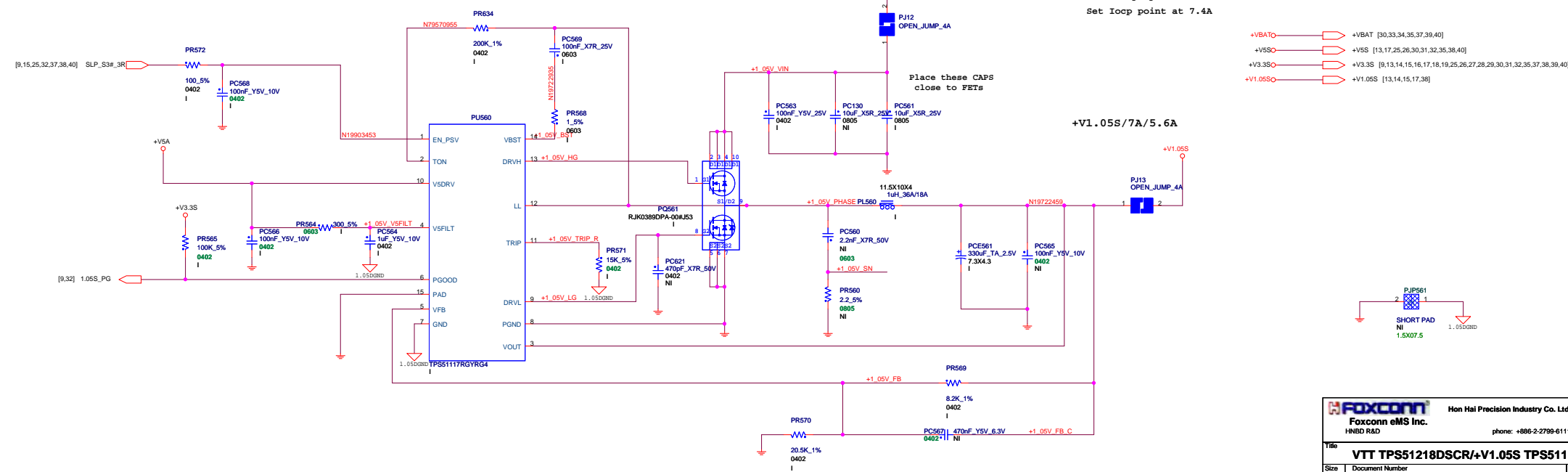


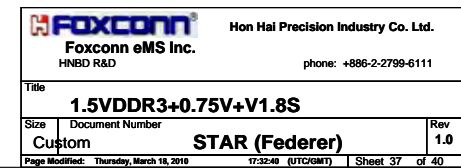
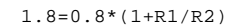
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Page Modified: Thursday, March 18, 2016		17:31:59 (UTC+8GMT) Sheet 35 of 40	

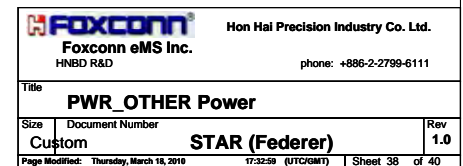
+VTT TPS51218



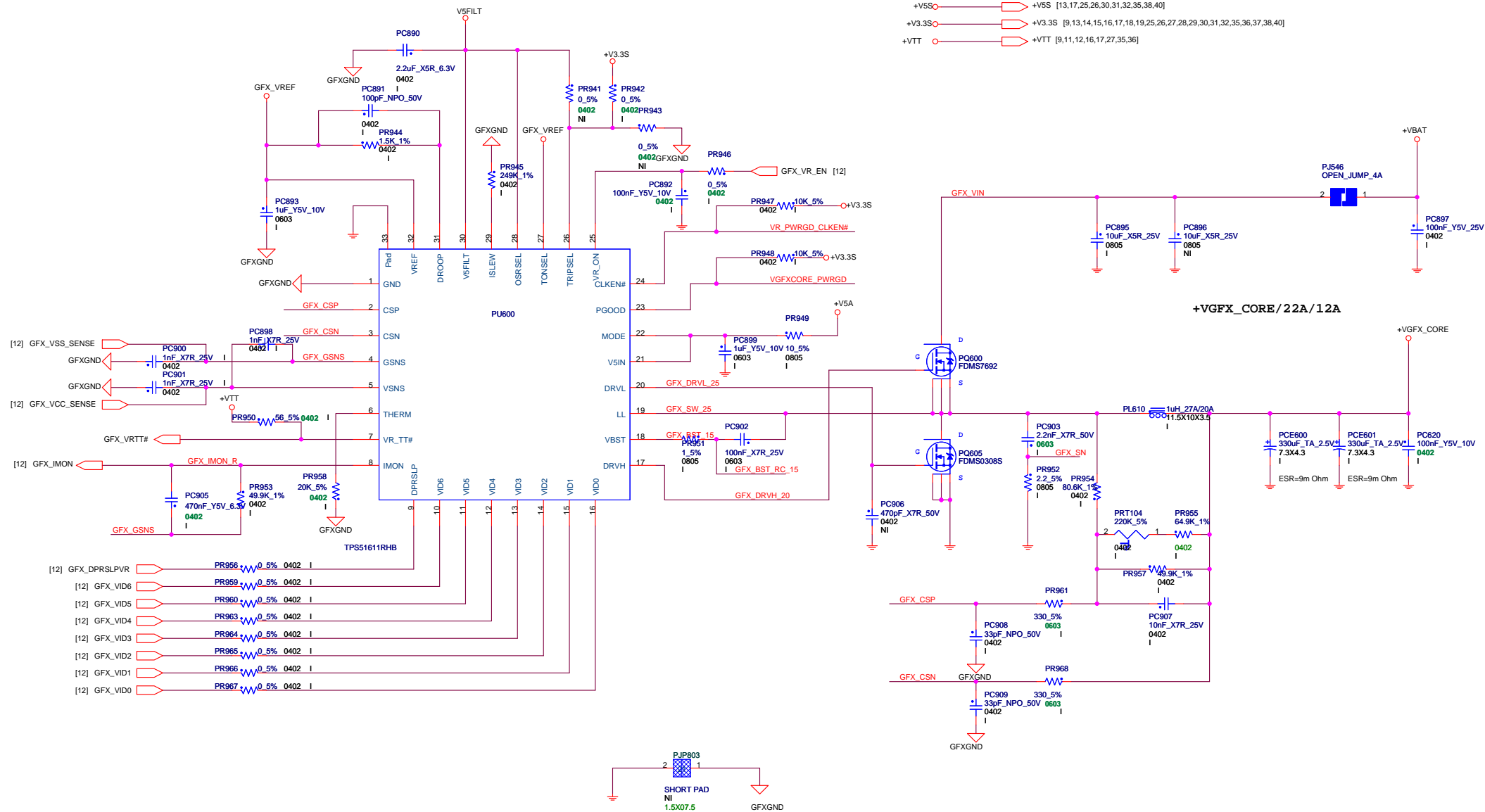
+V1.05S TPS51117

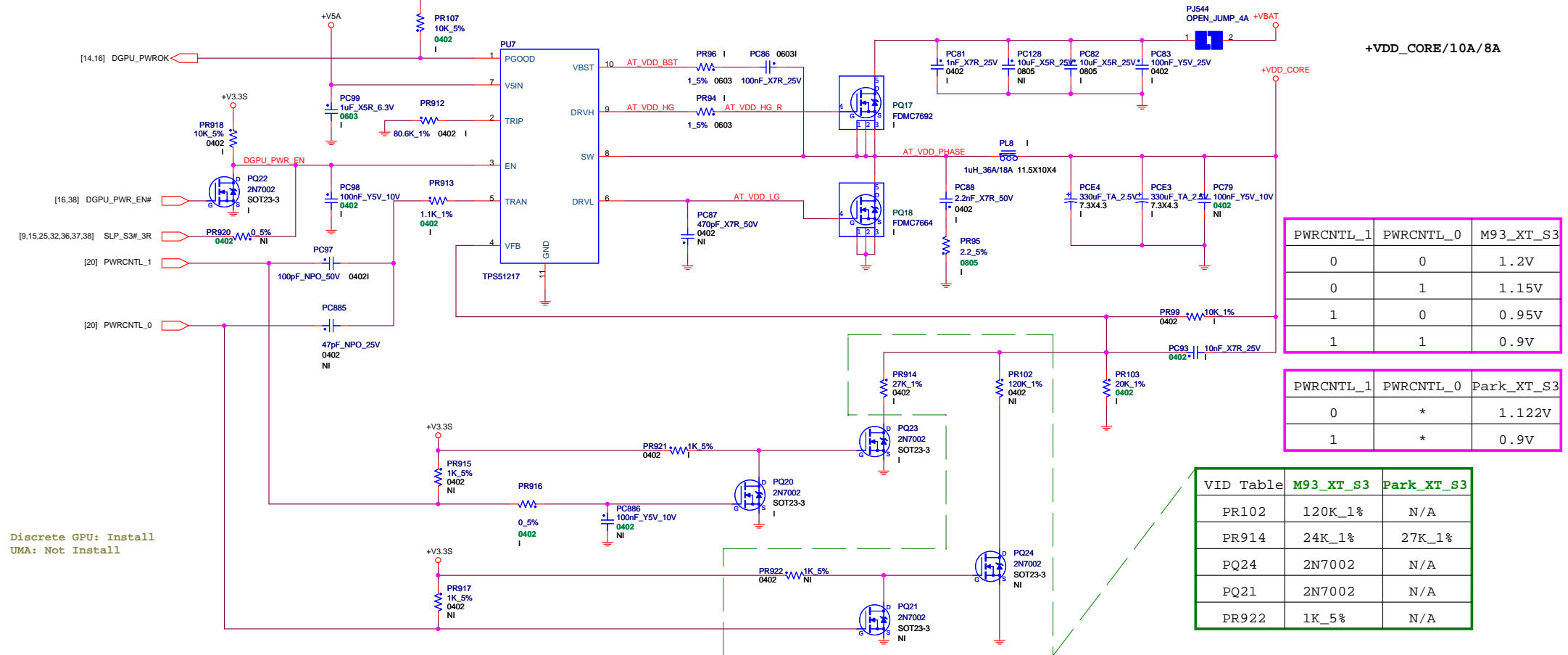




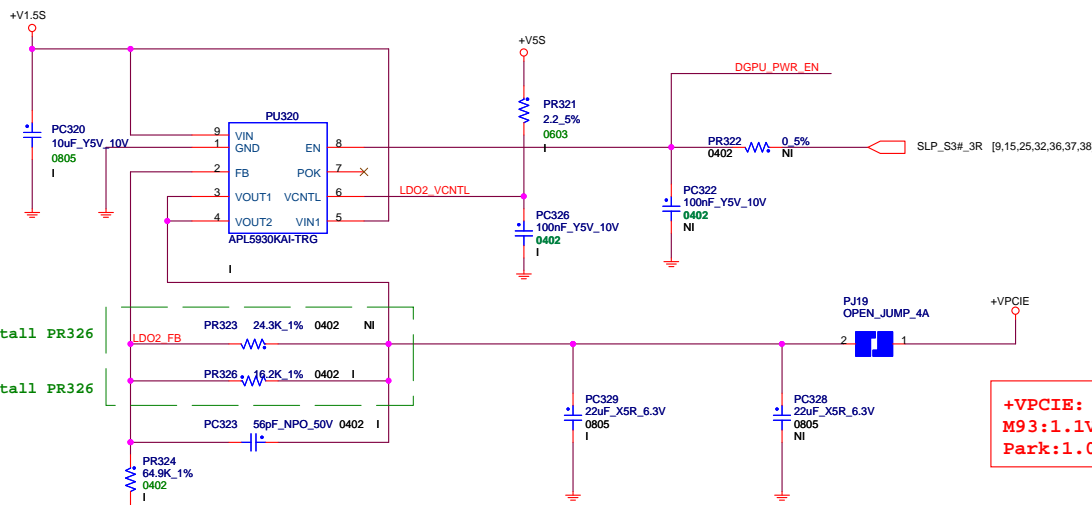


+VGFXCORE





Discrete GPU: Install
UMA: Not Install



M93-S3:
Install PR323 and Not Install PR326

Park-S3 :
Not Install PR323 and Install PR326

- +VBAT → +VBAT [30,33,34,35,36,37,39]
- +V5A → +V5A [17,26,29,34,36,37,38,39]
- +V5S → +V5S [13,17,25,26,30,31,32,35,38]
- +V3.3S → +V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,38,39]
- +V1.5S → +V1.5S [21,23,24,38]
- +VDD_CORE → +VDD_CORE [23]
- +VPCIE → +VPCIE [19,20,22,23]

+VPCIE:
M93:1.1V@150mA
Park:1.0V@125mA